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A Novel Structure of a Wideband Zero-bias Power Limiter for ISM Band

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Abstract

In this paper, a new broadband microwave microstrip power limiter is designed and realized. The Power Limiter is based on microstrip technology integrating a Zero Bias commercial Schottky diodes HSMS2820.The power limiter is optimized and validated in two steps. The enhanced and achieved circuit is obtained by concatenating two basic structures. The final circuit was validated into simulation by using ADS solver. Finally this circuit was realized and tested. Simulation and measurement results are in a good agreement. The final circuit achieves a limiting rate of 14 dB with a threshold input power level of 0 dBm until a maximum input power level of 30 dBm.

Keywords: *microstrip, power limiter, schottky diode*

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1. Introduction

The reliability of telecommunication systems and more generally of all electronic systems implies the use of powerful protection equipment to protect sensitive and expensive equipment from electric currents pulses [1-3] and high power signals [4-9]. Protective equipment, called Power Limiter, improves the stability of the protected system and avoids saturation situations that may affect the normal operation of the hall facilities.

In case of Microwave systems like radar, satellite system and telecommunication facilities, Power limiters are active microwave circuits used to protect sensitive devices such as LNA (Low Noise Amplifier) from the overloading of power signals and pulses. At low incident signal, the power limiter acts as a wave period with a small insertion loss. When the incident signal reaches the maximum power supported by the load, the power limiter must absorb or reflect some of the incident power in such a way that the load will see an incident signal with a constant power level below its peak limit. Thus, a power limiter is measured in a small signal to evaluate its insertion loss and measured with large power signal to evaluate its ability to dessipate the power beyond the threshold supported by the load to be protected. Figure 1 [10] shows a theortical response of a power limiter in three states: small signal, large signal and very large signal.

Most Microwave Power Limiters are designed by using solid state devices [4-10]. In literature, we found several techniques and solutions to achieve a solid state power limiters based especially on PIN diodes [5-8], Schottky diodes [9-12] and MESFET transistors [13-16]. Other solutions use superconducting [17], ferroelectric [18], ferro-magnetic [19-20] materials to achieve limiting behavior. There are also power limiters of gas-gap type [21-22] and mechanical limiters based on MEMS devices [23]. Power limiter can be classified in two types: active power limiters that require external current to operate and passive power limiters which are zero bias.

Solid state Power limiters (PL) are mainly based on the reflection and absorption of a portion of the input power. Among, the most basic topologies we have an example which is presented in Figure 2, the diode shunted between the transmission line and the common ground is used to limit the power level. When the power increases, the diode impedance decreases, and starts to absorb some of the received power and a rest of the power will be reflected [4].

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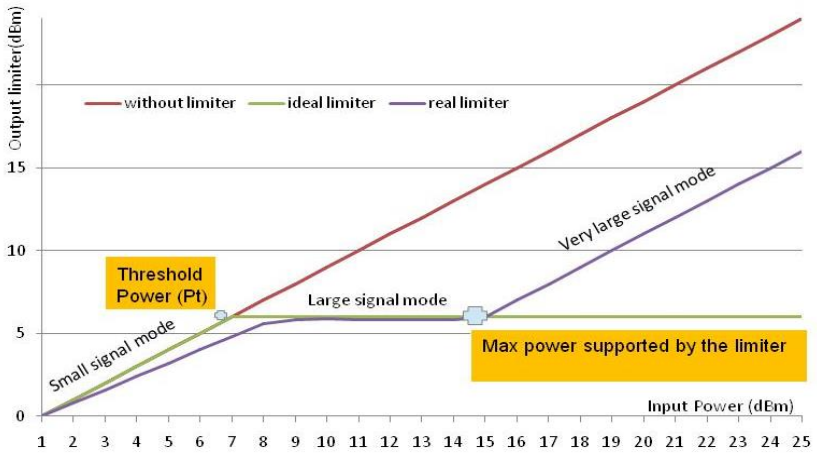


Figure 1. Output power vs Input Power

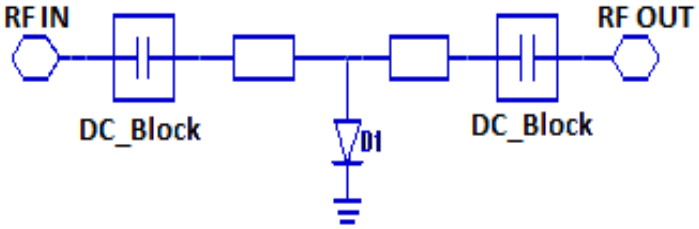


Figure 2. Classic power limiter topology

The classic toplogy presents certain limitations regarding insertion loss and bandwidth, especially when diodes are cascaded to improve the circuit limiting rate. To overcome these drawbacks, this paper deals with a new study on a novel structure of microwave power limiting which presents an originality concerning the wideband frequency and the use of zero bias diode which will limit the noise of the proposed circuit. In the following section, the new topology will be exposed and optimized, in section “realization results”, the results of real measurements will be presented and discussed.

2. Research Method

The proposed design is a passive power limiter based on two microstrip lines. One of them is a linear line that transmits the main signal and the second line is a ring line associated to two Schottky diodes. The ring line is used to divert a portion of incident signal when the amplitude of the signal reaches the threshold of the diodes. The two Schottky diodes operate as voltage controlled attenuator and current detector.

The designed circuit has been optimized in two steps by improving in each step the limiting rate while maintaining the insertion loss as minimum as possible. The final optimized circuit was realized and tested. Simulation and realized test results are compared and discussed.The structureof the proposed power limiter is presented in Figure 3.

For low signals, the characteristic impedance of the diodes is high. Consequently, the signal cannot pass through the ring line. The main line transmits the signal to the output with a low insertion loss generated mainly by the tangential line losses and capacitances of Schottky diodes junction. Yang et al. demonstrated in [24] that the insertion loss introduced by the one diode is approximated by {4.343*Rs (CjW)²*Zo} where Rs is its series resistance,Cj is its junction capacitance and Zo is the line impedance. Applying this approximation, it can be deduced that putting two diodes in series, as proposed in this paper, will reduce insertion loss by a ratio of 2.

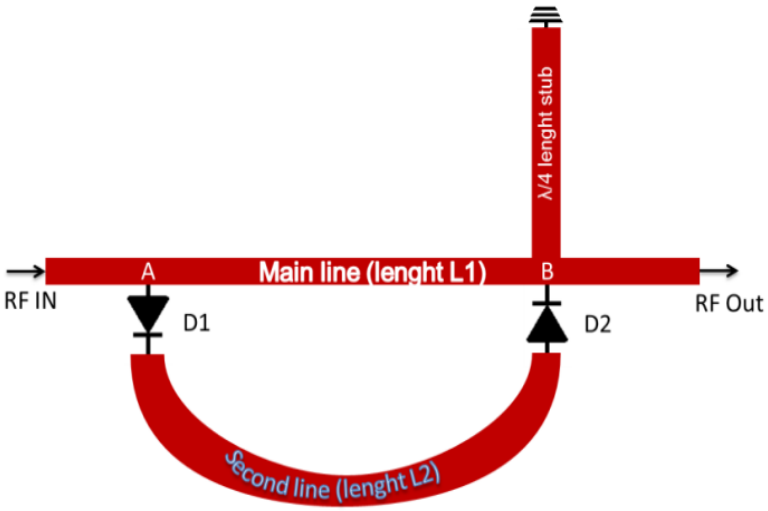


Figure 3. The structure of the new microstrip power limiter

In high signals, the received power exceeds the detection threshold of the Schottky diode. Consequently, the impedance of Schottky diode drops and the RF signal starts to spread on the ring line. Since the difference between the electrical length of the ring line and the main line is equal to λ/2, the signals propagating between the two lines will have a phase shift of π.

Schottky diode will generate a DC rectified current when it detects a high power signals. Therefore, an anti-parallel stub connected to the common ground is inserted to the main transmission line to assure the DC return path. The stub must have a quarter wave-lengths (λ/4) in order to provide an open circuit for high frequency and short circuit for DC current.

3. Equivalent Circuit of the New Design

As mentioned above, the commercial diode Avago HSMS2820 has been used in this circuit. This diode is a Surface Mount RF Schottky diode presented in SOT23/143 package [25] and suitable for incident power above -20 dBm. The HSMS282x family has been designed for RF applications [25], such as:

a. DC biased small signal detectors to 1.5 GHz
b. Biased or unbiased large signal detectors (AGC or power monitors) to 4 GHz
c. Mixers and frequency multipliers to 6 GHz.

The equivalent impedance of this Schottky diode, as depicted in Figure 4, is modeled as a combination of the variable junction resistance (Rj), the junction capacitance and parasitic series resistance (Rs):

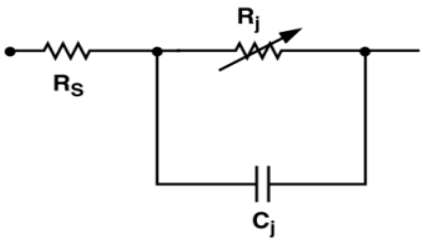


Figure 4. Linear equivalent circuit model of schottky diode

The equivalent circuit of the new design is presented above in Figure 5. The main line and the second line are replaced by LC circuit. The RF-Choke provides the return path for DC

current generated by diodes as self-rectified bias. To simplify calculations, we assume that the losses caused by the microstrip line are negligeables compared to losses caused by the junction resistance of the Schottky diodes.

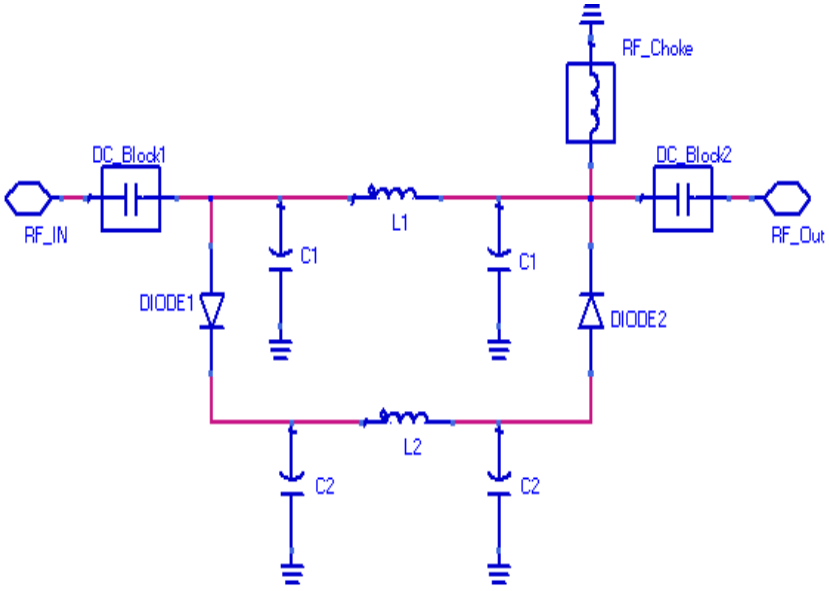


Figure 5. Equivalent power limiter circuit

To analyze this circuit, we can replace the topology in Figure 5 by the simplified diagram in Figure 6 where the impedance Ze is the equivalent impedance resulting from the setting in parallel between C1/L1 and Diode1/C2/L2/Diode2:

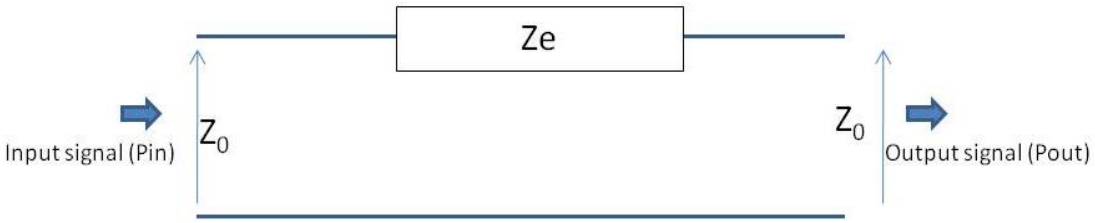


Figure 6. Simplified diagram of the power limiter circuit

the impedance Ze can then be written:

$$Ze = \frac{Z_1(Z_2 + 2Z)}{Z_1 + Z_2 + 2Z} \quad (1)$$

where Z_1 and Z_2 are the equivalent impedances of the main line and the secondary line respectively in the microstrip circuit, and Z is the equivalent impedance of Schottky diode. Since the difference between the electrical length of main line and the secondary line is equal to λ/2, the equivalent impedance of the two lines will have a phase shift of π. Thus Z1=-Z2. In consequence, the impedance Ze can be simplified as follows:

$$Ze = \frac{Z_1(Z_2 + 2Z)}{2Z} \quad (2)$$

As presented in [26], The ABCD matrix of the circuit presented in Figure 6 will be:

$$[ABCD] = \begin{pmatrix} 1 & Ze \\ 0 & 1 \end{pmatrix} \quad (3)$$

The conversion of ABCD matrix to scattering matrix as stated in [26-28] is used to calculate S21 and S11 as follows:

$$S21 = \frac{2}{2 + \frac{Ze}{Z_0}} \quad (4)$$

$$S11 = \frac{\frac{Ze}{Z_0}}{2 + \frac{Ze}{Z_0}} \quad (5)$$

In (4) and (5), we replace the impedance Ze by formula in (2) to express S21 and S11 by the values of Z, Z1, Z2 and Z0:

$$S21 = \frac{4.Z_0}{4.Z_0 + 2.Z_1 + \frac{Z_1.Z_2}{Z}} \quad (6)$$

$$S11 = \frac{2.Z_1 + \frac{Z_1.Z_2}{Z}}{4.Z_0 + 2.Z_1 + \frac{Z_1.Z_2}{Z}} \quad (7)$$

By analyzing (6) and (7), we find that:

a. If Z is very large, then S21 tends to $4Z_0/(4Z_0+2Z_1)$. This condition is realized when the diode is not biaised.
b. If Z is very small, then S21 tends to 0. This condition is realized when the diode is biaised.

In conclusion, for a small incident signal, the Schottky diode will presents a high impedance. Thus, the circuit will exhibit a low attenuation. On the contrary, in the large power signal, the impedance of the Schottky diodes drops and the circuit will exhibit a high attenuation.

In order to validate this theorical study by simulation in ADS software, and taking into account the junction capacity introduced by the Schottky diodes, we have set the following values for L1, C1, L2 and C2 as follows in Table 1.

Table 1. Lumped Circuit Values

Lumped Element	L1	C1	L2	C2
Value	18nH	0.2pF	8nH	0.2pF

Figure 7 presents the simulation results obtained in ADS.We can conclude that we have good matching input impedance between 2.2 GHz and 2.6 GHz. Figure 8 shows a characteristic output power versus input power. This behavior is very close to power limiter as presented in Figure 1. The power limiter presents a threshold input power value of 5 dBm.

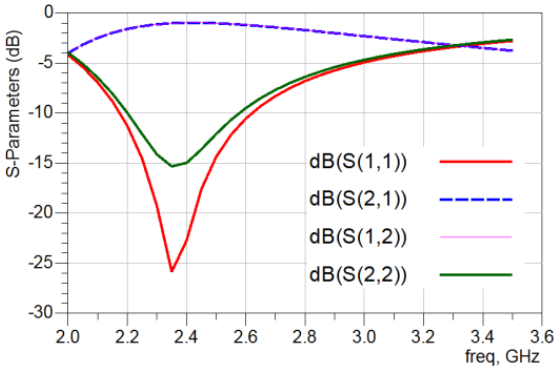


Figure 7. S-parameters results versus frequency

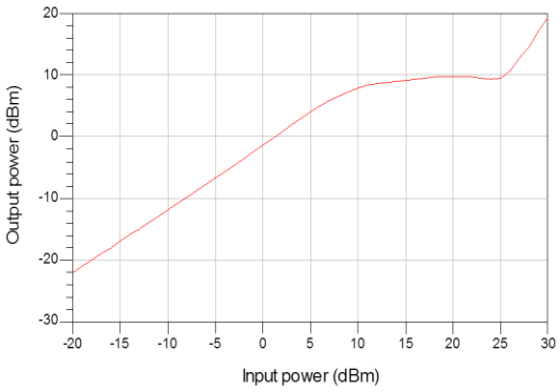


Figure 8. Limiting power characteristic output power versus input power

4. Circuit Validation by ADS Software

The designed circuit is mounted on an FR4 substrate with a relative dielectric constant value of 4.4 and a dielectric Loss tangent value of 0.025 and a thickness of 1.58 mm. The layout of the first circuit studied is presented in Figure 9. In this circuit we use one ring and two Schottky diodes HSMS2820. The Table 2 below presents the optimized dimensions of this circuit.

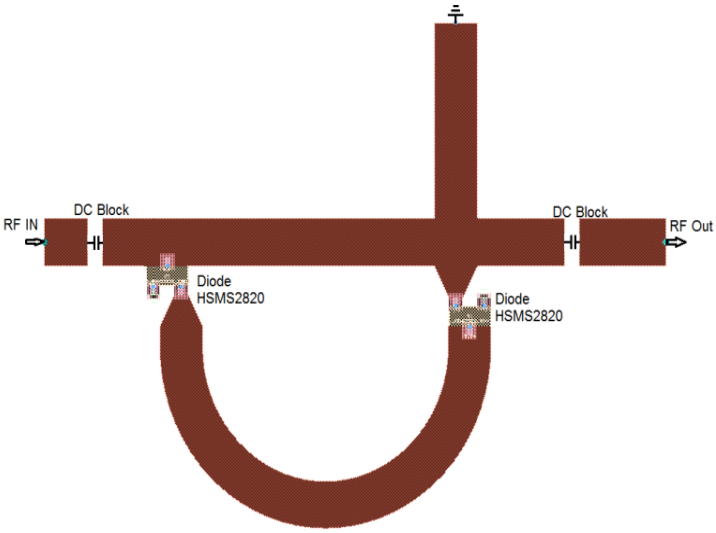


Figure 9. Layout of one ring circuit

Table 2. Dimensions of One Ring Circuit

Parameters	Values(mm)
Circuit length	46.16
Main line width	3
Ring line width	4
Ring line radius	11.58

The S-parameters simulation shows a good matching of the circuit over a bandwidth of 1 Ghz [1.6, 2.6 Ghz] with an insertion loss around -1 dB. However, the isolation reaches only 10dB at 30 dBm input power as presented in Figure 10.

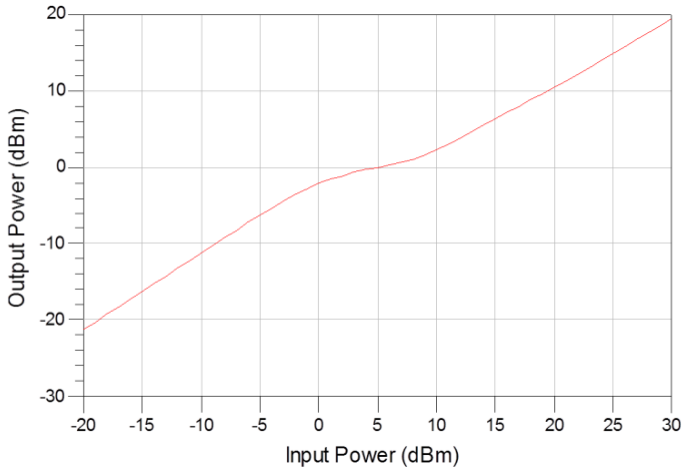


Figure 10. Output power versus input power

In order to improve the performances of this circuit, we have simulated a second circuit with two ring stages. The layout of the second optimized circuit is presented in Figure 11. The Table 3 presents dimensions of the two ring circuit layout.

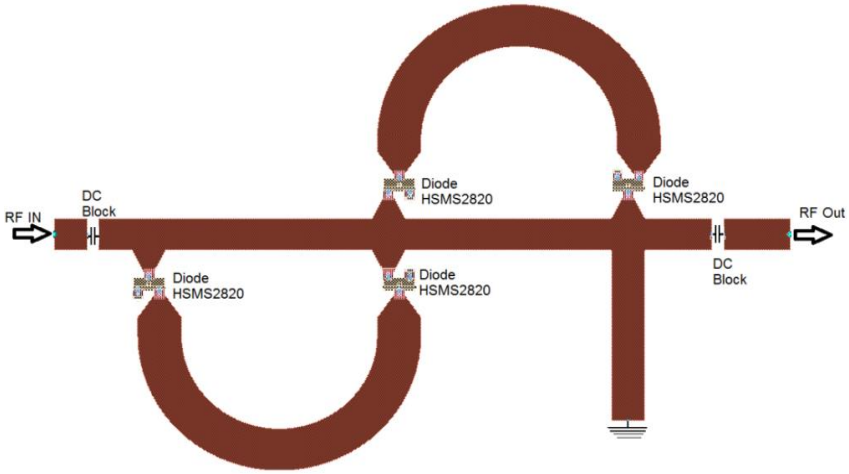


Figure 11. Layout of two stages ring

Table 3. Dimensions of two rings circuit

Parameters	Values(mm)
Circuit length	75
Main line width	3
Ring line width	4
Ring line radius	10.5

The insertion loss for low signal remains acceptable (around 1.3 dB). S-parameters simulation is presented in Figure 14 with the comparaison between simulated and measured results. The limitation power, as seen in Figure 12, is started when input power reaches 0 dBm. Depending on the operating frequency, the circuit provides 10 to 15 dB of attenuation for maximum input power level of 30 dBm.

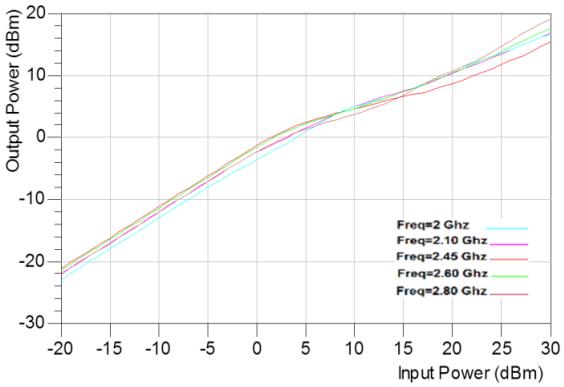


Figure 12. Output power versus input power for a sweep of frequencies

5. Circuit Fabrication and Measurement

After the validation of the proposed circuit into simulation, we have realized it at DICOM Laboratory in Cantabria University in Spain by using LPKF machine (a printed circuit board prototyping machine). The final achieved circuit is shown in Figure 13. Measurements have been carried out by using a microwave Vector Network Analyzer from Agilent technologies E8364A.

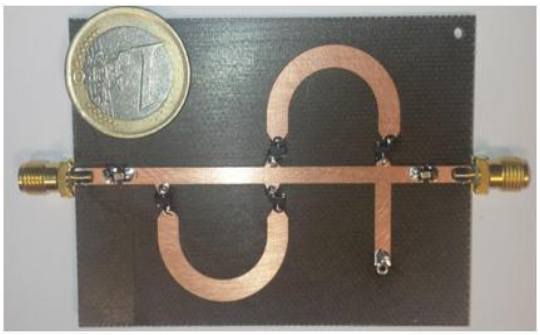


Figure 13. Realized circuit

6. Results and Discussion

Figure 14 presents a comparison between S-parameters simulation results and the measurements. As shown in the Figure 14, the realized circuit presents good matching input impedance between 1.9 GHz and 2.7 GHz. The measurements of reflection parameter (S11) and transmission parameter (S21) even have better results compared to the prediction of the simulation on the ADS software.

The improvement of the parameter S21 can be explained by the impact of the welding points and wire inductance of the diodes. This inductance contributes to the compensation of insertion loss introduced by the junction capacitance of the diode in small signal and consequently improves the adaptation of the circuit [24].

Large signal measurements are presented in Figure 15 for 1.9 GHz, 2.1 GHz, 2.3 GHz and 2.5 GHz frequencies. As seen in Figure 15, measurement and simulation are quite similar at low incident signal power (Pin < 0 dBm). While at high signal power, the measured output power slightly exceeds simulated power output. This difference is explained by the fact that parasitic inductance and capacitance of soldering are not included in the simulation parameters. However, the shape of the circuit response remains similar to a real power limiter as shown in Figure 1. In conclusion, the fabricated circuit shows a limiting behavior at input power threshold of 2 dBm with a maximum limiting rate of 14 dB.

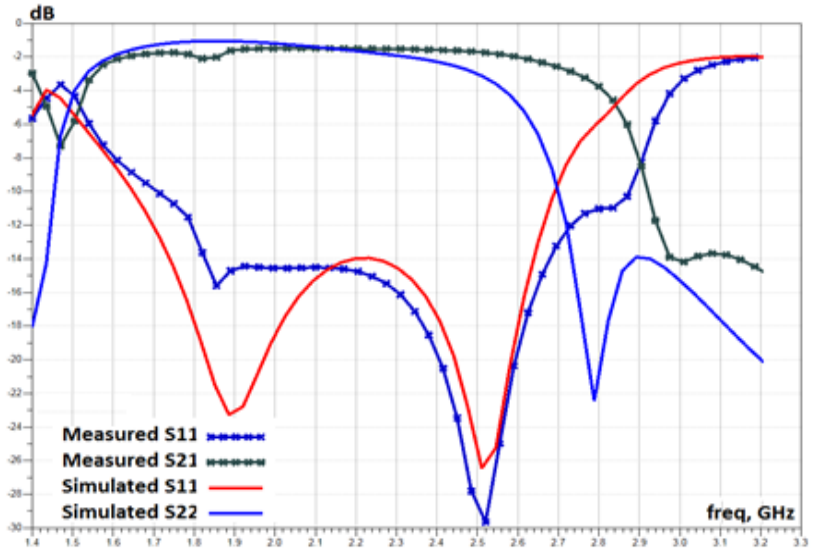
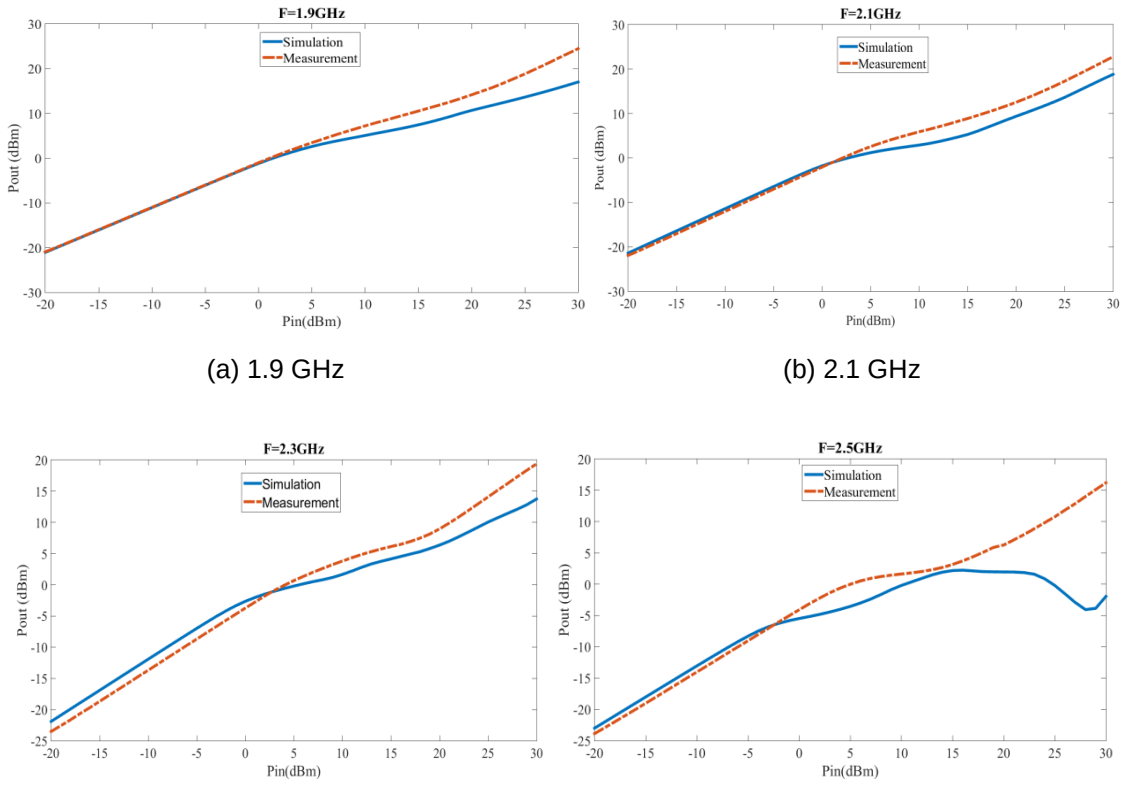


Figure 14. Simulated and measured results of S-parameters



(a) 1.9 GHz (b) 2.1 GHz

(c) 2.3 GHz (d) 2.5 GHz

Figure 15. Output power versus input power at (b) 2.1 GHz (c) 2.3 GHz (d) 2.5 GHz

7. Comparaison of Fabricated Circuit to Similar Studies in Litterature

In comparison to Power limiters topologies in literature, the designed circuit shows a simple and low cost solution for a passive power limiter based on Zero Bias Schottky diodes. The Table 4 presents a comparison between the proposed limiter and some power limiters validated in literature.

Table 4. Comparison of Microwave Power Limiter

Design	Insertion loss (dB)	Frequency range (Ghz)	Limiting rate (dB)	References
Microstrip Passive limiter using discrete Schottky diodes	1.3	2.45	14	The realized limiter
Passive limiter using PIN diode and detector diode	1.8 (simulation)	2.45	18 (simulation)	[11]
Monolithic limiter using Schottky didoe	1.5	0-20	15	[12]
Planar Schottky diode and MESFET based limiter	1	1	15	[13]
Passive limiter using Discrete MESFET and Schottky diode	0.9	7	15	[16]

In addition, the designed circuit shows important advantages in comparison to the state of art presented in literature:

a. The circuit presents simple construction by avoiding the need of external DC current and reducing the number of hole needed to connect the DC return path.
b. The use of zero bias diodes reduces Johnson noise caused by DC current and improves reliability of the circuit.
c. Schottky diodes present faster switching and RF power detections thus enhance circuit response to high power pulses [4].
d. The circuit uses less Schottky diode. For comparison, the design presented in [12] requires 6 HSMS2820 Schottky diodes to achieve a limiting rate of 15dB. The proposed broadband limiter uses only 4 Schottky diodes to deliver a similar limiting rate.

8. Conclusion

In this paper, we have designed, simulated and realized a power limiter circuit based on zero bias Schottky diode HSMS2820. The final circuit, using 4 Schottky diodes HSMS2820 implanted on two cascaded rings, permits to achieve 14dB of limiting power while the insertion loss at low signal remains acceptable (around 1.3 dB).

Compared to classic topology, the ring topology presents interesting advantages. Firstly it needs only one hole to connect the DC return path to the common ground, secondly it presents smaller dimensions of the circuit and needs only 4 Schottky diodes to achieve 14 dB of isolation.

The simulations and measured result permit to validate this microwave wideband power limiter for ISM band (industrial, scientific and medical band). The different steps followed to achieve such a circuit can be matched to propose another structure for other standards applications.

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